7. (Amended) The method according to Claim 5, wherein said electrically neutral material is implanted to a depth which is no greater than the depth of a diffusion region in said P-well.

REMARKS

In the July 6, 2001 Office Action, the Examiner has rejected claims 1, 2, 4 and 5 as being anticipated by Abiko et al. (EP 0 880 174 A1), and the Examiner has rejected claims 3, 6 and 7 under the provisions of 35 U.S.C. §103(a) as being unpatentable over Abiko et al. (EP 0 880 174 A1).

Claim 1 has been amended to include the feature of originally filed claim 6 (now canceled) relating to the step of "implanting an electrically neutral material into said substrate". Although, Abiko et al. (EP 0 880 174 A1) may disclose a trench and the implantation of boron ions, Abiko et al. clearly does not disclose the claimed step of amended claim 1 for implanting neutral material into a substrate after wells have been formed. Accordingly, amended claim 1 is not anticipated by Abiko et al., and the Examiner is respectfully requested to withdraw the rejection based upon 35 U.S.C. §102.

It is respectfully submitted that the prior art of record also does not teach, show or suggest that the claimed combination of amended claim 1 would be obvious to one of ordinary skill in the art. The Examiner has alleged in the Office Action that Gardner et al. (U.S. Patent No. 5,899,732) discloses implanting neutral material into a substrate after wells have been formed. Presumably, the Examiner is referring to Gardner's disclosure of the implantation of silicon for creating a gettering effect as being the implantation of a neutral material. Assuming for the purposes argument that the Examiner's allegation is correct, there is still no motivation to combine the teachings of Abiko et al. with the teachings of Gardner et al.

The stated purpose of implanting silicon in Gardner et al. is to create a gettering effect so that the region immediately beneath the junction is maintained at a lower dopant concentration to reduce junction capacitance. There is no teaching whatsoever that the implantation of Gardner et al should be performed in combination with the method of Abiko et al, nor is there any teaching whatsoever that the implantation of Gardner et al. will result in a radiation-tolerant integrated

circuit device, as claimed by the Applicant. Accordingly, it is respectfully submitted that the Applicants' amended claim 1 is patentable over the cited prior art. The Applicants further believe that dependent claims 2-5 and 7 are patentable over the cited prior art for at least the same reasons as independent claim 1 from which they depend.

The Applicants, therefore, respectfully submit that the amended claims are patentable over the prior art of record, and the Examiner is requested to pass the present application to issue.

Respectfully submitted,

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Appendix

1. (Amended) A method for fabricating radiation-tolerant integrated circuit devices, said method comprising:

depositing a layer of pad oxide on a semiconductor substrate;

selectively etching said pad oxide layer and said semiconductor substrate to define a trench within said semiconductor substrate; [and]

implanting boron ions at an angle with respect to normal in said trench; and

implanting an electrically neutral material into said substrate.

7. (Amended) The method according to Claim [6] 5, wherein said electrically neutral material is implanted to a depth which is no greater than the depth of a diffusion region in said P-well.